WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit, comprising:

voltage generation means for generating a voltage on the basis of control data loaded into a data register;

nonvolatile storage means for holding the control data; and

a processing circuit used to generate the control data held in said nonvolatile storage means, said processing circuit being formed on one semiconductor substrate together with said voltage generation means and said nonvolatile storage means,

wherein said processing circuit includes:

a decision circuit which determines a relationship between a deciding reference voltage supplied externally of the semiconductor substrate and the voltage generated by said voltage generation means; and

a control circuit which determines the control data on the data register by referring to an output from said decision circuit, and which stores the determined control data in said nonvolatile storage means from the data register,

and the operation of said control circuit is determined by a program.

2. The semiconductor integrated circuit according to claim 1, wherein said control circuit

performs, in response to a first operation mode, a processing for determining control data on the data register by referring to the output from said decision circuit and storing the determined control data in said nonvolatile storage means by reading out the data from the data register, and performs, in response to a second operation mode, a processing for loading the control data from said nonvolatile storage means into the data register.

3. The semiconductor integrated circuit according to claim 2, wherein said control circuit comprises a central processing unit.

4. The semiconductor integrated circuit according to claim 3, further comprising a random access memory accessible by said central processing unit,

wherein said central processing unit executes, in response to the first operation mode, a program held in a predetermined area of said random access memory.

5. The semiconductor integrated circuit according to claim 1, wherein said voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

6. The semiconductor integrated circuit according to claim 5, wherein said nonvolatile storage means comprises a flash memory, and said voltage generation means is capable of supplying a high voltage

for erasing or writing on the flash memory.

7. A semiconductor integrated circuit, comprising:

a plurality of nonvolatile storage elements electrically erasable and writable;

voltage generation means for generating a high voltage for erase and write on said plurality of nonvolatile storage elements on the basis of control data loaded into a data register from one of said nonvolatile storage elements; and

a processing circuit used to generate the control data held in said one of said nonvolatile storage elements, said processing circuit being formed on one semiconductor substrate together with said nonvolatile storage elements and said voltage generation means,

wherein said processing circuit includes:

a decision circuit which determines the relationship between a reference voltage supplied externally of the semiconductor substrate and the voltage generated by said voltage generation means; and

a control circuit which determines the control data by referring to an output from said decision circuit,

and the operation of said control circuit is determined by a program.

8. The semiconductor integrated circuit according to claim 7, wherein said control circuit

performs, in response to a first operation mode, processing for determining control data on the data register by referring to the output from said decision circuit and storing the determined control data in said one of said nonvolatile storage elements by reading out the data from the data register, and performs, in response to a second operation mode, processing for loading the control data from one of said nonvolatile storage elements into the data register.

9. The semiconductor integrated circuit according to claim 7, wherein said voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

10. The semiconductor integrated circuit according to claim 9, wherein said nonvolatile storage element is a flash memory element, and said voltage generation means is capable of supplying a high voltage for erase and write on the flash memory element.

11. A semiconductor integrated circuit, comprising:

a clock generation circuit which provides a clock signal having a signal cycle according to control data loaded into a data register;

nonvolatile storage means for holding the control data; and

a processing circuit used to generate the control data held in said nonvolatile storage means, said processing circuit being formed on one

semiconductor substrate together with said clock generation circuit and said nonvolatile storage means,

wherein said processing circuit includes:

a decision circuit which determines a relationship between the pulse width of a reference pulse signal and the pulse width of the clock signal generated by said clock generation circuit; and

a control circuit which determines the control data on the data register by referring to an output from said decision circuit,

and the operation of said control circuit is determined by a program.

12. The semiconductor integrated circuit according to claim 11, wherein said clock generation circuit includes an oscillation circuit, and a frequency dividing circuit which divides the frequency of an oscillation signal output from said oscillation circuit on the basis of the control data loaded into the data register.

13. The semiconductor integrated circuit according to claim 12, wherein said control circuit stores the determined control data in said nonvolatile storage means.

14. The semiconductor integrated circuit according to claim 13, wherein said control circuit performs, in response to a first operation mode, processing for determining the control data with reference to the output from said decision circuit and

storing the determined control data in said nonvolatile storage means, and performs, in response to a second operation mode, processing for loading the control data from said nonvolatile storage means into the data register.

15. The semiconductor integrated circuit according to claim 14, wherein said control circuit comprises a central processing unit.

16. The semiconductor integrated circuit according to claim 15, further comprising a random access memory accessible by said central processing unit,

wherein said central processing unit executes, in response to the first operation mode, a program held in a predetermined area of said random access memory.

17. The semiconductor integrated circuit according to claim 16, wherein the clock signal generated from said clock generation circuit is a write control clock signal; said nonvolatile storage means comprises a flash memory; and said write control clock signal determines the pulse width of a write pulse for writing to the flash memory.

18. A method of testing a plurality of semiconductor integrated circuits in a parallel manner, each semiconductor integrated circuit having voltage generation means capable of generating a voltage on the basis of control data loaded into a data register,

nonvolatile storage means in which the control data is held, a processing circuit used to prepare the control data held in the nonvolatile storage means, the processing circuit being formed on one semiconductor substrate together with the voltage generation means and the nonvolatile storage means,

a first process comprising a step of inputting a reference voltage to the plurality of semiconductor integrated circuits from the outside in a parallel manner; and

second process comprising the steps of: in execution of a test operation by means of the processing circuit of each semiconductor integrated circuit, determining a relationship between the voltage generated by the voltage generation means and the reference voltage on the basis of control data set in the data register; updating the control data until a target condition is reached by the determination result; and storing the control data in the nonvolatile storage means when the target condition is reached by the determination result.

19. The method of testing a plurality of semiconductor integrated circuits according to claim 18, further comprising a third process including loading a test program into each semiconductor integrated circuit,

wherein said second process includes making said determination by using a decision circuit in the

processing circuit; and making a central processing unit in the processing circuit execute the test program to update the control data and to store the control data in the nonvolatile storage means.

20. The method of testing a plurality of semiconductor integrated circuits according claim 18, wherein the voltage generation means comprises a boosting circuit which boosts a power supply voltage externally supplied.

21. The method of testing a plurality of semiconductor integrated circuits according to claim 20 wherein the nonvolatile storage means comprises a flash memory, and the voltage generation means is capable of supplying a high voltage for erase and write on the flash memory.

22. A method of testing a plurality of semiconductor integrated circuits in a parallel manner, each semiconductor integrated circuit having an oscillation circuit, a frequency dividing circuit which controls the ratio of division of the frequency of an oscillation signal output from the oscillation circuit on the basis of a control data loaded into a data register, nonvolatile storage means for storing the control data, and a processing circuit used to generate the control data held in the nonvolatile storage means, said processing circuit being formed on one semiconductor substrate together with the oscillation circuit, the frequency dividing circuit, and the

nonvolatile storage means, comprising:

a first process comprising the step of instructing each of the plurality of semiconductor integrated circuits to execute a test operation; and

a second process comprising the steps of: in execution of the test operation by means of the processing circuit of each semiconductor integrated circuit, determining a relationship between the pulse width of a periodic signal generated by the frequency dividing circuit and the pulse width of a reference pulse signal on the basis of the control data set in the data register; updating the control data until a target condition is reached by the determination result; and storing the control data in the nonvolatile storage means when the target condition is reached by the determination result.

23. The method of testing a plurality of semiconductor integrated circuits according to claim 22, further comprising a third process comprising the step of loading a test program into each semiconductor integrated circuit,

wherein said second processing comprises the steps of making said determination by using a decision circuit in the processing circuit; making a central processing unit in the processing circuit execute the test program to update the control data and to store the control data in the nonvolatile storage means.